CMPUT 329 - Computer Organization and Architecture II
Final Exam — Fall 2003

Prof. José Nelson Amaral
Computing Science Department
University of Alberta

Name:

CMPUT 329 Honor Code

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Edmonton, December 15, 2003.

Question 1	/20
Question 2	/15
Question 3	/30
Question 4	/15
Question 5	/20
Total	/100
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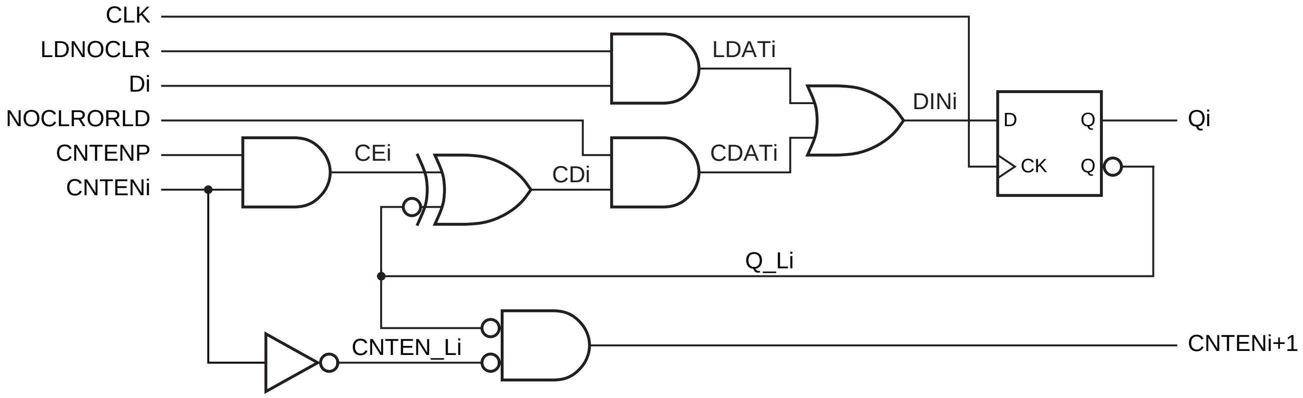

Figure 1: One bit-cell for a 74x163-like counter. (From J. F. Wakerly, pp. 8-45).

Question 1 (20 points): Boolean Algebra and Circuit Analysis

Figure 1 displays a one bit-cell for a synchronous serial counter that operates in a fashion similar to the 74x163 counter.

a. (**10 points**) Write the boolean expression for the signal `DINi`. Write an expression that reflects exactly the circuit shown in Figure 1. Do not do any simplification.

b. (**10 points**) Write the most simplified canonical sum of products expression for `DINi`.

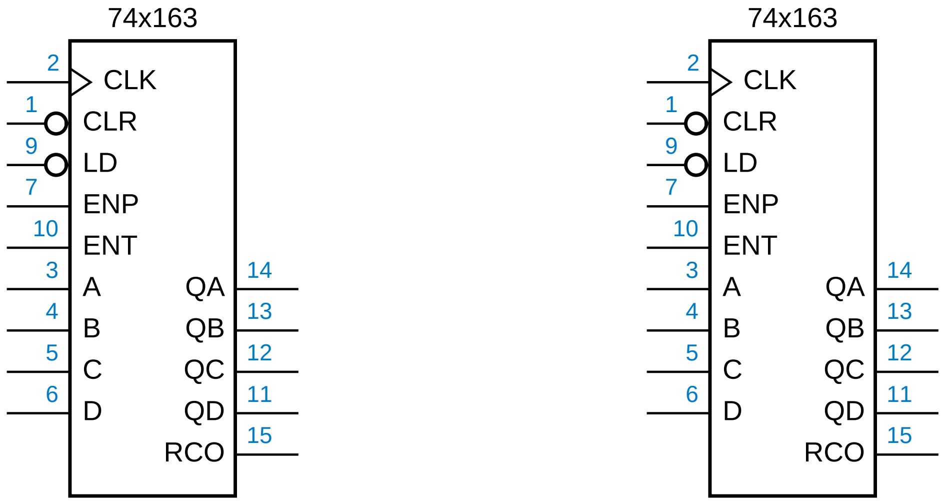

Figure 2: 74x163 Counters.

Question 2 (15 points): Designing Counters (From J. F. Wakerly, pp. 789)

In the design of a digital device you need to implement a module-129 counter. You have space for two `74x163` circuits, and you have only a single inverter available to complete the design. Show, in Figure 2 how you will connect the two `74x163` and the inverter (if necessary) to implement the module-129 counter. Figure 3 shows the state table for the `74x163`. Remember that the RCO output is 1 when all outputs (`QA, QB, QC, QD`) are 1.

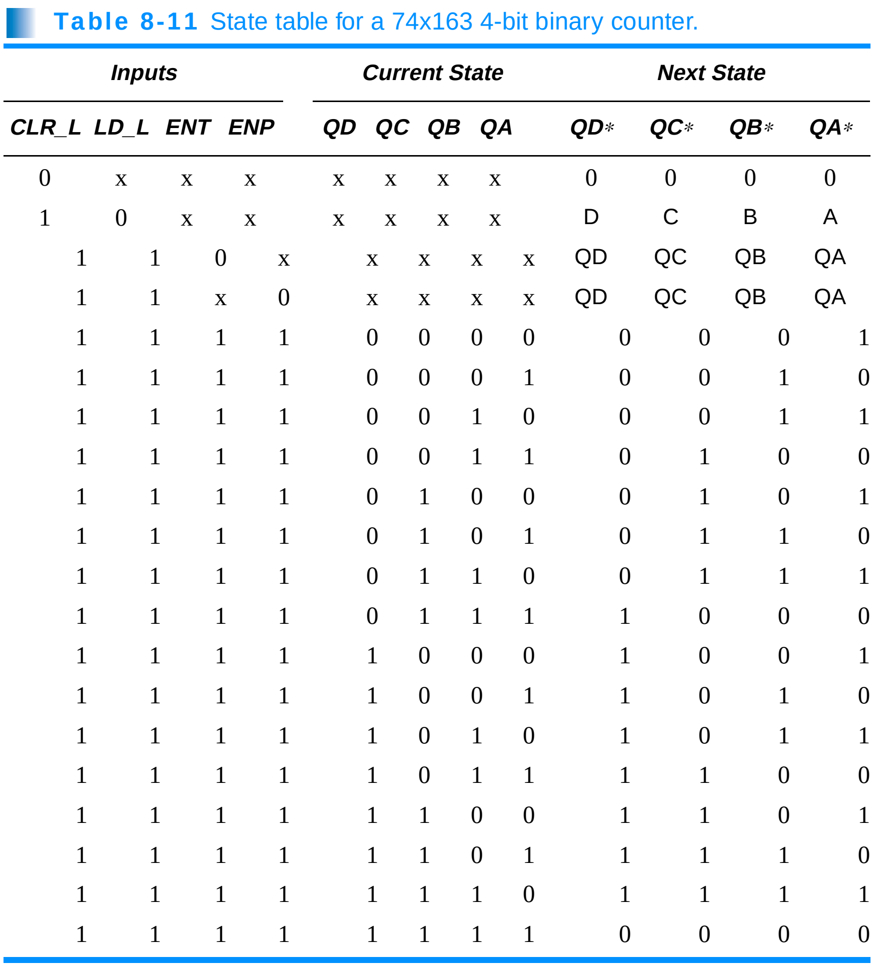

Table 8-11 State table for a 74x163 4-bit binary counter.

Inputs				Current State				Next State			
CLR_L	*LD_L*	*ENT*	*ENP*	*QD*	*QC*	*QB*	*QA*	*QD∗*	*QC∗*	*QB∗*	*QA∗*
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

Figure 3: State table for a 74x163 4-bit binary counter.

Question 3 (30 points): Sequential Design (From D. D. Givone, pp. 388)

A serial adder has two one-bit inputs, `a` and `b`, and one one-bit output, `sum`. When the circuit is turned on it goes automatically to the reset state for which the value of an internal carry-in bit is zero. After the circuit is turned on, two N digit number are inputted sequentially into `a` and `b`, one bit per clock cycle. The `sum` output produces, one cycle late, the value of the sum. The following table illustrates the operation of the serial adder. This sequence of inputs and outputs are the sum of the value `A = 00110100` with the value `B = 00110110` producing the result `SUM = 01101010`. Note that the bits are inputed in reverse order. Also `sum` is outputting the result of the addition of the inputs seen in the previous clock cycle along with a carry bit generated by lower significant bits. The circuit continues operating in this manner forever. Thus to start a new addition we need to be sure to input enough zeros to reset the value of the carry-in bit to zero.

Clock Cycle	0	1	2	3	4	5	6	7	8
a	0	0	1	0	1	1	0	0	X
b	0	1	1	0	1	1	0	0	X
sum	0	0	1	0	1	0	1	1	0

In a Moore machine the current outputs are a function only of the current state. You are asked to design a Moore machine to implement the serial adder described above.

Your answer will be evaluated according to the following criteria.

a. (**10 points**) A finite state diagram or a state table with the minimum number of states, and a clear description of the meaning of each state.

b. (**5 points**) An appropriate state assignment that results in a reasonable set of excitation equations. We are not asking for an optimal state assignment, but we do expect you to produce a reasonable one. You should clearly list your state assignment into a separate table. Explain why you chose the state assignment that you used. (Hint: Once you have decided how many states and how many bits you need, decide which states should be close to each other. Then you can use a Karnaugh map to find which binary combinations are close to each other).

c. (**5 points**) A clearly drawn state transition table that can be read easily.

d. (**5 points**) Clearly drawn and correct Karnaugh maps for an implementation of the sequential circuit with D type flip-flops.

e. (**5 points**) Correct minimal canonical sum-of-products form excitation and output equations for the finite state machine.

Continuation of Question 3

Question 4 (15 points): State Minimization (from C.H. Roth Jr., pp. 417)

In this question you will work with the following state table:

Present	Next State		Present Output	
State	`X=0`	`X=1`	`X=0`	`X=1`
a	h	c	1	0
b	c	d	0	1
c	h	b	0	0
d	f	h	0	0
e	c	f	0	1
f	f	g	0	0
g	g	c	1	0
h	a	c	1	0

a. (**10 points** Reduce the state table to a minimum number of states.

b. (**5 points**) You are given two identical circuits that realize this state table. One circuit is initially in state "c" and the other network is initially in state "f". Specify an input sequence of length two which could be used to distinguish between the two networks, and give a corresponding output sequence from each network.

Question 5 (20 points): Memory Technology

In very brief sentences, state what is the main characteristic of each one of the memory types below.

a. (**2 points**) Random Access Memories (RAMs)

b. (**2 points**) Static Random Access Memories (SRAMs)

c. (**2 points**) Dynamic Random Access Memories (DRAMs)

d. (**3 points**) Fast Page DRAMs

e. (**3 points**) Extended Data Output DRAM (EDO-DRAMs)

f. (**3 points**) Synchronous DRAMs (SDRAMs)

g. (**2 points**) Double Data Rate SDRAMs (DDR-SDRAMs)

h. (**3 points**) Rambus DRAMs (RDRAMs)